REMARKS

Claims 1-17 are pending in this application. Claims 1, 9 and 15 have been amended. No new matter has been added.

Claim Rejections under 35 U.S.C. §103

Claims 1-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamada, U.S. Patent No. 5,986,924 in view of Houston, U.S. Patent No. 6,611,451, Sim et al., U.S. Patent No. 6,456,555 and Ohbayashi et al., U.S. Patent No. 6,556,058. Applicants request reconsideration and reexamination of the rejection in view of the foregoing amendments and for the following reasons.

Applicants have amended claims 1, 9 and 15 to set forth the source potential control circuit of the invention as having at least first and second elements connected in parallel to each other, with the first element having a resistance less than a resistance of the second element and the first element having a resistance that is predetermined according to a value of V_{th} of the MOSFETs. Support for the amendment is found in the specification from page 13, line 17 to page 15, line 13, for example.

As amended, each of the independent claims sets forth that there are a switch, or equivalent, and a source potential control circuit between the source line and the ground potential, and further that the source potential control circuit has first and second elements. Accordingly, the amended independent claims are supported by the disclosure of the three elements set forth in the drawings, such as the switch (SW1), resistance (R1), or transistor having a normally on-state, and diode (M1) connected between the source line ss1 and the ground potential line ss as shown in Figure 1, for example. According to the invention, when the threshold voltage V_{th} of a transistor varies toward a lower value, the elements of the switch and source potential control circuit are operated to reduce the leakage current due to the fact that the leakage current of the transistor at the on-state and the source line potential increases.

In Yamada, an SRAM, which is disclosed in the prior art of Figure 12, is shown to have a plurality of SRAM cells each having the driver MOSFET, transfer MOSFET,

load MOSFET, switch transistor and resistor. Accordingly, Yamada discloses a device between a source line and a ground potential line comprised of a switch and a resistor connected in parallel to each other. Applicants note that Houston discloses a device between the source line and a ground potential line comprised of a switch and a diode connected in parallel to each other. However, neither Yamada or Houston, nor any of the references of record, disclose the combination of a switch and a source potential control circuit connected between a source line and a ground potential wherein the source potential control circuit includes at least first and second elements, as claimed by Applicants. Further, the references do not suggest the combination of Yamada and Houston proposed by the rejection.

In particular, Yamada discloses that the leakage current may be reduced because the current passing through a resistance is increased with an increase of a leakage current and a source line potential is increased due to an increase of the potential of both sides of the resistance. However, the arrangement in Yamada poses a problem in that the source line potential may be increased more than an expected value, thereby causing data in the memory cells to be damaged or lost. To prevent this problem in the present invention, the source potential control circuit has a second element connected in parallel with the first element, such as a diode in addition to the resistance. The diode, as is well known, does not allow a current to flow until a potential at both sides reaches a predetermined value, and once the current starts to flow, the potential at both sides does not continue to increase. Accordingly, the diode has a function of determining the upper limit of the potential. The characteristics of the diode can prevent an excessive increase in the source line potential by providing an upper limit of the source line potential at the state of a low V_{th} (high leakage current). On the other hand, without including a device performing a diode function, the increase in the source line potential may become excessive and damage data in the cells.

In the situation where the variation of V_{th} of a transistor varies toward a higher value, the sources line potential is not required to increase because of the decrease in the leakage current of the transistors at the off-state. Further, the source line potential can be set to a value so as to reduce the leakage current while being sufficiently high so as to

avoid damage of the data in the memory cells. See page 15, lines 4-13 of the specification, for example.

With respect to Houston, which discloses a switch and a diode connected in parallel to each other between a source line and ground potential line, without a resistance, the diode provides the characteristic in which an excessive increase of the source line potential can occur, and even when the leakage current is not critical, the value of the source line potential can increase to an extent at which the memory cells are likely to be damaged. Neither Yamada nor Houston discloses or suggests the combination of a switch and a source potential control circuit that includes first and second elements connected in parallel to each other, all being connected between the source line and the ground potential, as claimed by Applicants. Each of Yamada and Houston teaches to one having ordinary skill in the art that the leakage current should be reduced by increasing the source potential by connecting a diode or a resistance with a switch in parallel between the source line and ground potential. That is, the result of the teachings of Yamada and Houston is to include a device in parallel with the switch that increases the source potential. Accordingly, the combination of Yamada and Houston does not disclose the combination set forth in the amended independent claims in which the switch is connected between a source line and a ground potential with a source potential control circuit that includes first and second elements connected in parallel to each other.

Sim is cited for disclosing diode-connected MOS transistors that are used as resistors. In Ohbayashai, an n-channel MOS transistor is disclosed as constituting a resistance element. Neither Sim nor Ohbayashai makes up for the deficiencies in the Yamada and Houston references with respect to the subject matter claimed in the independent claims, however. Further, each of the dependent claims is patentable at least for depending from a base claim and further each is patentable over the art of record. Accordingly, in view of the foregoing arguments, the rejection of claims 1-17 under 35 U.S.C. §103(a) as being unpatentable over Yamada, U.S. Patent No. 5,986,924 in view of Houston, U.S. Patent No. 6,611,451, Sim et al., U.S. Patent No. 6,456,555 and Ohbayashi et al., U.S. Patent No. 6,556,058 should be withdrawn.

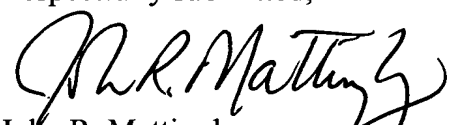
Request for Continued Examination

Applicants have filed a Request for Continued Examination (RCE) in order to ensure entry and consideration of the amendments made to the claims since this application is under final rejection.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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